AMENDMENTS TO THE CLAIMS

88. (New) A processor for operating certain data in accordance with an instruction, comprising:

a first register unit for holding data;

a second register unit for holding data; and

a processing unit for processing at least zero-extending data when the instruction designates the first register and for processing at least sign-extending data when the instruction designates the second register.

89. (New) The processor of claim 88, wherein the instruction includes a destination operand which designates either the first register unit or the second register unit.

90. (New) The processor of claim 89, wherein the data is an immediate data.

91. (New) A data processing method for executing an instruction that designates one of a first register and a second register, said method comprising the steps of:

decoding the instruction;

processing at least zero-extending data when the instruction designates the first register; and

processing at least sign-extending data when the instruction designates the second register.

92. (New) The method of claim 91, wherein said instruction includes a destination operand which designates either the first register unit or the second register unit.

93. (New) The method of claim 92, wherein said data is an immediate data.

94. (New) The processor for executing instructions, comprising:

a first register unit for holding data;

a second register unit for holding data;

a first processing unit for processing zero-extending data; and

a second processing unit for processing sign-extending data,

wherein an instruction can direct the first processing unit to perform zero-extending when the instruction designates the first register unit and can direct the second processing unit to perform sign-extending when the instruction designates the second register unit.